REMARKS

Claims 1-6 are all the claims pending in the application. By this Amendment, Applicants amend claims 1-4 to better conform them to U.S. patent practice.

Claim Rejections - 35 U.S.C. § 112

Claims 5 and 6 are rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. For *at least* the following reasons, Applicants respectfully traverse the rejection.

Applicants respectfully submit that claims 5 and 6 are supported by the Applicants' disclosure. Claim 5 recites that the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed. It is alleged in the Office Action "[t]is is new material introduced in the current amendment and is not allowed". See Office Action, pages 2 and 3, paragraph 3.1. Applicants respectfully disagree.

For example, *at least* page 7, line 22 to page 8, line 6 of the Specification, and FIGS. 3-5 of the Applicants' drawings support the above-noted features of claim 5. FIG. 3 is a waveform diagram showing the rise and fall delay patterns of a 2-input AND circuit, according to a non-limiting, exemplary embodiment of the present invention. That is, FIG. 3 is an example of the claimed delay time information in the delay analysis library. In the case where the input 1 rises and the input 2 falls, the Specification discloses that "no terminal is selected for delay analysis" (Specification, page 8, lines 5 and 6). That is, when no change in a signal state of an output

terminal of the logical circuit is determined (see FIG. 3, middle column – 'Rise/fall'), the delay analyzing module determines that no further delay analysis needs to be performed. Moreover, this determination is necessarily automatic since it is based on the logical operation information of the logical circuit, which is stored in the delay analysis library. Therefore, Applicants respectfully submit that claim 5 complies with the requirements of 35 U.S.C. § 112.

Applicants further submit that the features of claim 6 are supported by the Applicants' disclosure. For example, claim 6 recites that the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case. It is alleged in the Office Action "[t]is is new material introduced in the current amendment and is not allowed". See Office Action, pages 3 and 4, paragraph 3.2. Applicants respectfully disagree.

For example, Applicants respectfully submit that the portions of the Specification and Applicants' drawings discussed above with respect to claim 5 also support the features of claim 6. It appears that the Examiner's position is that since the claim features at issue are allegedly

not found explicitly in the Applicants' Specification, the subject claim limitations must not be supported by the Applicants' disclosure. Applicants respectfully submit, however, that there is no *in haec verba*—i.e., word for word—requirement for satisfying the written description requirement. Therefore, contrary to the Examiner's assertions, Applicants are not burdened to show where the claimed terms are explicitly recited in the Specification. Rather, the newly added claim limitations can be supported in the Specification through express, implicit, or inherent disclosure (*Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997 as cited in MPEP § 2163.02). Additionally, Applicants can show possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. *Id.*

Here, in a non-limiting, exemplary embodiment of the claimed delay time information shown in FIG. 3, it is shown in the middle column of the table in FIG. 3 (the 'Rise/fall' column) that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals. Further, it is shown that at a time at which the second clock signal among the two clock signals is input, the state is LOW which is the same state as the first signal state (i.e., at the first clock signal). Accordingly, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to the clock signal (see Specification, page 8, lines 5 and 6), and thus, in this case the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate. Therefore, the delay analyzing module, based on this delay time information,

automatically determines that no further delay analysis needs to be performed as recited in claim 6. *Id.* As such, Applicants respectfully submit that claim 6 complies with the requirements of 35 U.S.C. § 112.

Claim Rejections - 35 U.S.C. § 101

Claims 1-3, 5, and 6 are rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. For *at least* the following reasons, Applicants respectfully traverse the rejection.

Applicants do not acquiesce to the rejection of claims 1, 2, 5, and 6. In order to expedite prosecution, however, Applicants amend the claim to recite "A delay analysis system, executed on a computer, for making a delay analysis..." It is asserted in the Office Action that "[t]he specification as originally filed does not describe the system to include a computer apparatus. Therefore this claim cannot be patented under 35 USC 101. This amounts to functional descriptive material without having functional and structural relationship to otherwise statutory machine". See Office Action, pages 4 and 5, paragraphs 5.1 and 5.2. Applicants respectfully disagree.

Applicants respectfully submit that the Specification clearly envisions hardware components to enable the functions to be realized by the delay analysis system set forth in claim 1 or 2. For instance, referring to a non-limiting, exemplary embodiment of the present invention, the Specification states that the "delay analysis system according to the present invention...may be implemented by a computer-executable program" (Specification, page 5, lines 9-13). Moreover, Applicants respectfully submit that *any* software must execute on hardware to

perform the functions set forth by the claimed delay analyzing module of claims 1 and 2. As such, Applicants submit that claims 1 and 2 comply with the requirements of 35 U.S.C. § 101.

Claims 5 and 6 are patentable *at least* by virtue of their dependency.

With respect to method claim 3, it is alleged in the Office Action that "the method comprises two steps of referencing a delay analysis library and selecting a delay time from delay time information in the library. A method listing mental steps is not patentable unless the method is implemented in a computer or an apparatus or transforms some material or article into a different state or thing. The application does not describe anywhere computer implementation of the method and does not show or describe a computer for implementing the method. Therefore this claim cannot be patented under 35 USC 101". See Office Action, page 6, paragraph 5.3, emphasis added. Applicants respectfully disagree.

Applicants respectfully submit that, as discussed above with respect to claims 1 and 2, the Specification does provide support for computer implementation of the claimed method contrary to the assertions in the Office Action. In particular, as noted above, the Specification states that the "delay analysis system according to the present invention...may be implemented by a computer-executable program" (Specification, page 5, lines 9-13). Clearly then, the method may be implemented on a computer (e.g., see claim 4). Accordingly, Applicants respectfully submit that claim 3 complies with the requirements of 35 U.S.C. § 101.

Claim Rejections - 35 U.S.C. § 103

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hasegawa (U.S. Patent No. 6,041,168) (hereinafter Hasegawa '168) in view of Hasegawa (U.S.

Patent No. 5,528,511) (hereinafter Hasegawa '511). For *at least* the following reasons, Applicants respectfully traverse the rejection.

In the previous Amendment, it was submitted that there is no delay time information in Hasegawa '511 which is **specific to** an input terminal logical **state transition** (e.g., at input terminals 's' or 'v', see FIGS. 4 and 5) and a resulting logical **state transition** at an output terminal (e.g.,, at output terminal 't'), as required by claim 1. Moreover, it was submitted that the delay times shown in FIGS. 12 and 13 of Hasegawa '511 are identified between the input terminals 's' or 'v' and the output terminal 't'. On the other hand, with the configuration set forth in claim 1, a target point at which no further delay analysis is required is automatically determined (see previous Amendment, page 7, last paragraph to page 8, first full paragraph).

In response, in the current Office Action, the Examiner contends that "**Hasegawa** '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa** '511 discusses at CL1, L28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa** '511 states at CL2, L30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa** '511 describes at CL3, L5-26 that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are

modified. Therefore, **Hasegawa** '511 teaches a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (CL2, L61-65)" (Office Action, page 17, first full paragraph). Applicants respectfully disagree.

For instance, the invalidness specifier indicated by the invalidness specification in FIG. 7 of Hasegawa'511 is not, and cannot be, automatically generated unlike the delay time information of claim 1. This is because in Hasegawa '511, the "OR DEVICE" of FIG. 2 is not always an OR device, and moreover, there is no information provided in Hasegawa's alleged delay analysis library of what logical circuit is the subject of the delay analysis. Specifically, Hasegawa '511's FIG. 3 is merely one example, which does not form the basis that the information of FIG. 7 is correct in all cases. Thus, **manual** judgment is necessary for preparing the information indicated by the invalidness specifier of FIG. 7. On the other hand, in the present invention as claimed, the delay analysis library already comprises logical operation information which in turn comprises the delay information of the logical circuit, based on which the delay analyzing module can automatically analyze the delay of the logical circuit (e.g., the delay analyzing module, based on the delay time information, can generate indicative information that an action is invalid or valid). Hasegawa '511, alone, or in combination with Hasegawa '168, does not teach or suggest this feature.

In view of the foregoing, Applicants respectfully submit that claim 1 is patentable over the alleged combination of Hasegawa '168 and Hasegawa '511.

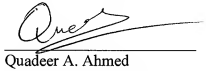
Claims 2-4 recite features similar to those discussed above with respect to claim 1. Therefore, claims 2-4 are patentable for *at least* reasons similar to those given above with respect to claim 1.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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